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# (54) CLOCK REGENERATION CIRCUIT

(57) Abstract

PROBLEM TO BE SOLVED: To provide a clock regeneration circuit in which frequency synchronization can be performed without exerting an adverse influence upon a clock regeneration part.

SOLUTION: The clock regeneration circuit is provided with clock regeneration means (1-8) and frequency detecting means (9-14) and by using an edge counter 11 for frequency detection for frequency synchronization, error output provided by a digital controller oscillator(DCO) 8 and the edge counter 11 becomes a 0th-order error not to be integrated. Even when a phase shift occurs in a regenerated clock, just a single frequency occurs and errors do not continuously occur.